IN THE UNITED STATES PATENT OFFICE

Applicants:	Brian T. Brunn et al.		
Assignee:	Xilinx, Inc.		
Title:	BIT-EDGE ZERO FORCING EQUALIZER		
Serial No.:	10/791,924	File Date:	March 2, 2004
Examiner:	Siu M. Lee	Art Unit:	2611
Docket No.:	X-1549 US	Conf. No.:	3818

Mail Stop AMENDMENT
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, Applicants bring to the attention of the Examiner the reference listed in the attached form PTO/SB/08B. A copy of the reference will be included with this submission.

Citation of the listed reference shall not be construed as an admission that the reference is necessarily prior art with respect to the instant invention. Citation of the listed reference shall not be construed as a representation that a search has been made other than as described above. Also, citation of the listed reference shall not be construed as an admission that the information cited herein is, or is considered to be, material to patentability as defined in §1.56(b).

This submission is being filed after receipt of a first Office action. Accordingly, the Commissioner is authorized to charge the $180 filing fee for this matter to Deposit Account No. 24-0040.

Respectfully submitted,

Michael R. Hardaway
Attorney for Applicants
Reg. No. 52,992

I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent & Trademark Office on February 25, 2008.

By: Susan Wiens
Susan Wiens

MRH:slw